

REMARKS

Claims 1-6 are pending in the application. Claims 1-3 have been amended and claims 7-11 have been added, leaving claims 1-11 for consideration upon entry of the present Amendment. As will be discussed in detail below, it is believed that the application is in condition for allowance.

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al. (US 6,420,200) ("Yamazaki") in view of Arai (US 6,369,507) and Takayama et al. (US 5,986,632) ("Takayama"). For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art and that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996).

Claim 1, as amended, includes the following limitation: "the contact position between the wiring layer and the thin film transistor is placed to be distant from the contact position between the wiring layer and said element to be driven in the horizontal direction and outside the formation region of said first electrode in the horizontal direction." Accordingly, the claim requires that the contact position is placed outside the formation region of the first electrode in the horizontal direction. Yamazaki, Arai, and Takayama do not teach or suggest that limitation.

Figures 2 and 14 of Yamazaki show that the contact positions between the wiring layer 37 and the thin film transistor 202 is formed below the first electrode 46 or 51, and thus, the contact position is not outside the formation region for the first electrode, as recited in claim 1. In fact, Yamazaki teaches that the contact position and an end of the first electrode 46 are approximately on the same position in the vertical direction, and therefore, the contact position is immediately below the formation region of the first electrode 46.

The advantage of locating the contact position outside the first electrode is that the emissive layer can be formed as flat as possible. It is desirable to have as flat a surface as possible for the formation surface of the emissive layer so as to improve the reliability of the emissive element.

Moreover, Arai teaches that a wiring electrode or the like and an organic EL layer are disposed on the same plane, and do not constitute a layered structure as recited in claim 1. In Takayama, there is no disclosure of the connection structure between a driving element and an EL element. As such, Yamazaki, Arai, and Takayama, either alone or in combination, do not teach or suggest all of the limitations of claim 1.

Accordingly, because none of the references teach or suggest all of the limitations in claim 1, Applicant respectfully requests that the rejection be withdrawn.

Claim 2 includes the following limitation: "at least a portion of the contact hole region and at least a portion of said first electrode are filled with a flattening layer; and said emissive element layer and said second electrode are formed above said flattening layer." Claim 3 includes the following limitation: "at least a portion of a recess of said first electrode covering said contact hole is covered by a flattening layer; and said emissive element layer is formed above said flattening layer." Yamazaki, Arai, and Takayama do not teach or suggest that limitation.

First, Yamazaki does not teach or suggest that that at least a portion of the first electrode is filled with a flattening layer or that the flattening layer covers the first electrode. Yamazaki teaches that the flattening layer 44 is located below the first electrode 46 or 51. See Figures 2 and 14 of Yamazaki.

Moreover, the reason for the flattening layer 44 of Yamazaki is different than the reason for the flattening layer in claims 2 and 3. The flattening layer in claims 2 and 3 is present because of the contact hole. Yamazaki teaches that the reason for the flattening layer is to flatten the step caused by the thin film transistors. Column 7, lines 64-67 explain that the insulation layer 44 is formed to flatten the step, which has been caused by the plurality of thin film transistors. As such, because the flattening layer 44 flattens the step in the thin film transistors, it must be located directly above the thin film transistors and not the first electrode.

Moreover, Arai and Takayama do not teach or suggest those limitations. As such, Yamazaki, Arai, and Takayama, either alone or in combination, do not teach or suggest the limitations of claim 1. Accordingly, because none of the references teach or suggest the limitations in claims 2 and 3, Applicant respectfully requests that the rejection be withdrawn.

In addition, claim 4 includes all of the limitations of claim 1, claims 5 and 6 include all of the limitations of claims 2 and 3, respectively. As such, the rejection as to claims 4-6 should also be withdrawn.

Applicant has also added claim 7, which includes all of the limitations of claim 2. Thus, for the reasons discussed above with respect to claim 2, Applicant respectfully requests that claim 7 be allowed. In addition, claim 7 includes the following limitation: "the contact position between the wiring layer and the thin film transistor is placed outside the formation region of said first electrode in the horizontal direction." This limitation is similar to the limitation described above with respect to claim 1 in that the limitation requires that the contact position is placed outside the formation region of the first electrode. Accordingly, for this additional reason, claim 7 should be allowed.

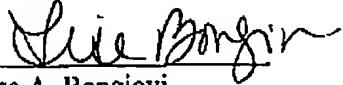
In addition, claims 8-11 are allowable. Those claims include the limitation: "at least a portion of a recess of said first electrode created due to said second contact hole is filled with a flattening layer; and said emissive layer and said second electrode are formed above said flattening layer and said first electrode." As explained above, none of the references teach or suggest that limitation. In addition, claim 9 also includes the following limitation: "the contact position between the wiring layer and the thin film transistor is placed outside the formation region of said first electrode in the horizontal direction." As explained above with reference to claim 1, none of the references teach or suggest that limitation. Accordingly, Applicant respectfully requests that claims 8-11 be allowed.

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicant's attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

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